

PGallery 2.0 + Demo 1. Coaster
Classic 2.0.5.1 Crack IStripper
Virtual Strip Club CRACK
IStripper. 3. HijackThis-Pro-9-Cr
ack-Keygen-2.8.1-Full-Version-
with-Regtotmp-Parallelr-License-
Key-Full-Uni.rar Malwarebytes
Anti-Malware Premium
5.12.2.2060 + License
Key.torrent. In order to achieve
a low-output, a high efficiency,
and a high-density in a large-
scale integrated circuit, a fine

pattern such as a gate electrode, a gate insulating film, and a diffusion layer or an interconnection must be formed with a high accuracy. This requires a technique for forming the fine pattern with high accuracy. For this purpose, a stepper (exposure apparatus) is used. In the stepper, a semiconductor wafer as a workpiece is placed on a wafer chuck (workholding table) and fine patterns are transferred and formed on the

wafer by using a photomask (reticle) having an opening pattern corresponding to each of the fine patterns to be formed. An alignment mark (alignment mark) is formed on the semiconductor wafer. Fine positions of the photomask and the semiconductor wafer are adjusted to correct misalignment of the fine patterns to be formed on the wafer. A conventional technique in which an alignment mark is formed on a

semiconductor wafer for alignment and the alignment mark is detected by using an image processing technique is disclosed in Japanese Patent Application Laid-Open No. 2001-93985 (Patent Document 1). In this technique, it is necessary to properly set a light source position for exposure in order to improve the alignment accuracy. For this purpose, the light source position is adjusted while detecting the alignment mark

by using the image processing technique, in which a margin for adjustment is assured. That is, the light source position is shifted while taking into consideration the margin for the adjustment. This margin for the adjustment is not a margin for a displacement itself of the alignment mark. However, when an alignment error occurs, the margin for the adjustment is reduced in the technique described in Patent Document 1. This may reduce

the alignment accuracy and lower the accuracy for alignment of fine patterns on a semiconductor wafer. In addition, the margin for the alignment may be set smaller to improve the alignment accuracy 6d1f23a050

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